ABSTRACT

A disk controller includes memory that is accessible by both a microprocessor and hardware parity logic. Parity-related operations are identified by scenario, and parity coefficient subsets are stored in a memory table for each different parity-related

5 calculation scenario. To perform a particular parity-related operation, the microprocessor determines the operation's scenario and identifies the corresponding coefficient subset. The hardware parity logic is then instructed to perform the appropriate parity computation, using the identified coefficient subset. In one embodiment, parity segments are calculated by a parity segment calculation module

10 that is embodied as an application specific integrated circuit (ASIC). The ASIC includes one or more result buffers for holding intermediate computation results, one or more mathematical operator components configured to receive data segments and coefficients associated with the data segments and operate on them to provide intermediate computation results that can be written to the one or more result buffers,

15 and one or more feedback lines. The feedback lines are coupled between an associated result buffer and an associated mathematical operator component and provide an intermediate computation result to the math operator for use in calculating parity segments.